34.5 Redefinition of Write Margin for Next-Generation SRAM and Write-Margin Monitoring Circuit

Koichi Takeda[1], Hidetoshi Ikeda[1], Yasuhiko Hagihara[1], Masahiro Nomura[1], Hiroyuki Kobatake[2]

[1]NEC, Sagamihara, Japan
[2]NEC Electronics, Kawasaki, Japan

To help overcome the speed limits of the conventional SRAM, a 7T-SRAM was previously developed [1], an 8T-SRAM was also proposed [2]. While these SRAMs have the advantage that the threshold voltage (V_{th}) of SRAM cell transistors can be lowered to achieve high-speed operations, they still have the same need for improved writability as conventional SRAMs do. With decreases in supply voltage (V_{DD}) and increases in the transistor mismatch accompanied by the geometric scaling, write margin (WM) and read margin deteriorate. SRAM power-supply control schemes have been proposed to improve WM [3, 4], but values obtained with the conventional WM definition are meaningful only when WM is low, and measurements need to be done under worst-case PVT conditions. The impact of V_{th}-deviation, temperature, and supply voltage on WM also need to be measured under worst case. This severely increases the time required to develop SRAMs. In this paper, a new definition is proposed for WM, one in which it is inversely proportional to transistor mismatch over a wider range of PVT values; a WM-monitoring circuit based on this definition is also presented.

In the SRAM cell shown in Fig. 34.5.1, when the BL signal is set to 0, the NMOS transistor (N3) is turned ON, which results in a voltage drop in the storage node holding data 1. This is the trigger for write operations to begin. Stable write operations require that the current of N3 be higher than that of PMOS transistor P1. Because of the importance of N3 in write operations, there should be a correlation between the WM value and the N3 drivability under all conditions. Conventional WM is expressed as a butterfly curve based on the respective dc characteristics of the two inverters in the SRAM cell [5]. In order to test the validity of conventional WM values, Monte-Carlo simulations are performed. The figure illustrates 32,000 points. In consideration of the possibility of future advances in process technologies, simulation conditions are based on an assumed σV_{th}=50mV. For V_{DD}=1.0V, there is no correlation between WM values and ΔV_{th} of N3. For V_{DD}=0.75V, a correlation appears only after ΔV_{th} of N3 exceeds 0.14V.

Figure 34.5.2 illustrates the newly defined WM. In SPICE simulations of the dc characteristics of Inverter-1, the WL is used as the Inverter-1 input terminal. The input to n2 of Inverter-1 is V_{OL}, the lowest voltage level of the output of Inverter-2. Since the output of Inverter-2, V2, will not be reversed until the output of Inverter-1, V1, reaches the logical threshold voltage (V_{TH}) of Inverter-2, the margin 0V state is assumed to occur when Inverter-1 output V1 equals V_{TH} of Inverter-2. Here, the voltage level of WL for the case of margin 0V is referred to as V_{WL}. Since the maximum voltage level of WL is V_{DD}, WM may be defined as the difference between this V_{DD} and V_{WL}, (V_{DD}-V_{WL}). As shown in Monte-Carlo simulation results, a -1.0 correlation appears for both V_{DD}=1.0V and V_{DD}=0.75V. Further, for all SRAM cells, a change from 1.0V to 0.75V results in a drop in WM of roughly 161mV. In addition, there is a correlation between the conventional WM and the proposed WM where WM values are low. This confirms the validity of the proposed definition.

Monte-Carlo simulations are also performed to evaluate the effects of WM improvement technology. As shown in Fig. 34.5.3, during write operations, the SRAM power supply value, VDD_SRAM, is maintained at V_{DD2}, which is lower than V_{DD} [3]. The current of P1 decreases, which makes conditions for stable write operations easier to meet. While conventional WM values improve only in SRAM cells where ΔV_{th} of N3 exceeds 0.14V, the proposed WM values of all SRAM cells improve by about 81mV when V_{DD2} is decreased.

Figure 34.5.4 shows the proposed WM-monitoring circuit based on the proposed WM definition. An opamp controls the input voltage level of N3, V_{WL}, so that the voltage levels of nodes n1 and n2 become equal. Inverter-2 is used to reverse the output of Inverter-1. Inverter-3 outputs V_{OL} to P1 in Inverter-1. WM values are obtained by subtracting V_{WL} from V_{DD}. SPICE simulation results show the settling time of the WM-monitoring circuit to be 0.5ns. A decrease from 1.0V to 0.75V in V_{DD} results in a decrease of 159mV in WM, and a decrease from 0.75V to 0.65V in V_{DD2} results in 78mV improvement in WM .

In order to further test the proposed WM definition, the WM-monitoring circuit is implemented in a 90nm CMOS test chip (Fig. 34.5.7). Figure 34.5.5 shows measurement results for 2,432 SRAM cells in four SRAM macros with different average V_{th} values. With a conventional WM definition, although WM distribution would be a normal distribution, WM would be independent of average V_{th}. With the proposed WM definition, WM distribution is also a normal distribution, and WM improves with decreasing V_{th} in the SRAM cell transistor, as expected. By increasing PMOS $|V_{th}|$, WM is further improved. Since there is a linear relationship between the proposed WM and transistor mismatch, and since transistor-mismatch distribution is a normal distribution, measurement results can be extrapolated to the Y-axis (WM = 0), and there is no possibility that the WM value fall below 0V in 90nm Mb-scale SRAMs. If, however, in consideration of the possibility of future advances in process technologies, transistor mismatch were to be doubled, the WM value at standard deviation = -6σ could fall below 0V. While, with conventional 6T-SRAMs, it is necessary to apply at least one of the WM improvement technologies described in [3] and [4], with 7T- and 8T-SRAMs, WM can be improved simply by decreasing the V_{th} of SRAM-cell transistor. The WM-monitoring circuit is also evaluated. A decrease from 1.0V to 0.75V in V_{DD} results in about 135mV drop in WM, and a decrease from 0.75V to 0.65V in V_{DD2} results in about 63mV improvement in WM .

The proposed WM-monitoring circuit can be applied in SRAM power-supply circuits for WM improvement [3]. Figure 34.5.6 shows V_{th} margin windows for generation, in which σVth is 50mV. The windows are simulated for a V_{th} variation of 5σ in each SRAM cell. V_{th} values lying within the gray areas are useable. The upper limit of NMOS V_{th} is roughly 0.4V. If, as an example, 2GHz operations were to be required, the upper limit of PMOS $|V_{th}|$ would be roughly 0.5V, limited by the rising time of the storage node (write speed limit 2). A 0.1V decrease in V_{DD2} improves the upper limit of NMOS V_{th} by 40mV, but degrades the upper limit of PMOS $|V_{th}|$ by 40mV. This is caused by a decrease in PMOS transistor drivability. The proposed WM-monitoring circuit is needed in order to set V_{DD2} to the maximum voltage at which WM will be sufficient.

Acknowledgments:
We are grateful to Masao Fukuma, Naotaka Sumihiro, and Naoki Nishi for their very important encouragement and support.

References:
[1] K. Takeda, et al., "A Read-Static-Noise-Margin-Free SRAM Cell for Low-VDD and High-Speed Applications," *ISSCC Dig. Tech. Papers*, pp. 478-479, Feb., 2005.
[2] L. Chang, et al., "Stable SRAM Cell Design for the 32 nm Node and Beyond," *Symp. VLSI Tech.*, pp. 128-129, June, 2005.
[3] K. Zhang, et al., "3-GHz 70Mb SRAM in 65nm CMOS Technology with Integrated Column-Based Dynamic Power Supply," *ISSCC Dig. Tech. Papers*, pp. 474-475, Feb., 2005.
[4] M. Yamaoka, et al., "Low-Power Embedded SRAM Modules with Expanded Margins for Writing," *ISSCC Dig. Tech. Papers*, pp. 480-481, Feb., 2005.
[5] W. J. Dally and J. W. Poulton, "Digital Systems Engineering," Cambridge University Press, 1998.

 1-4244-0079-1/06/$20.00

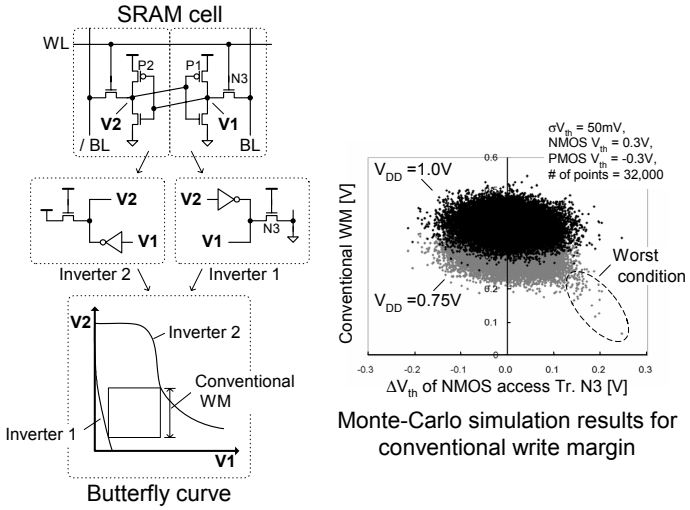

Figure 34.5.1: Conventional write margin.

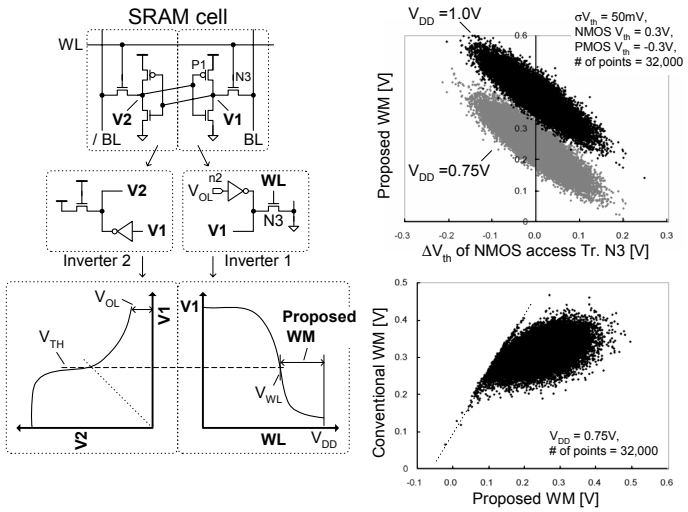

Figure 34.5.2: Proposed write margin.

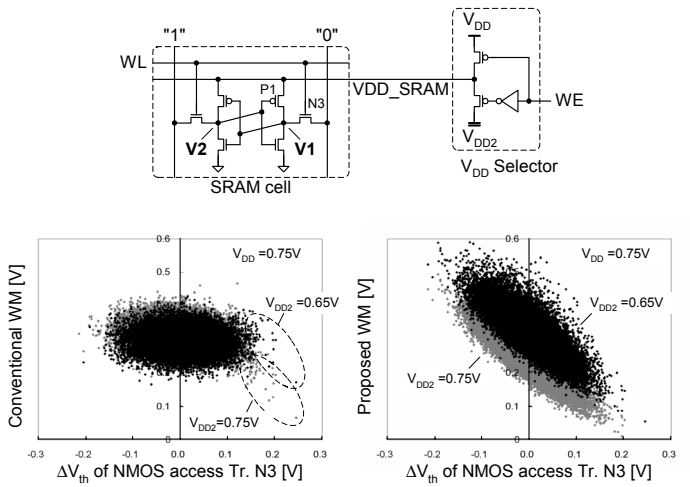

Figure 34.5.3: Conventional write-margin improvement technology.

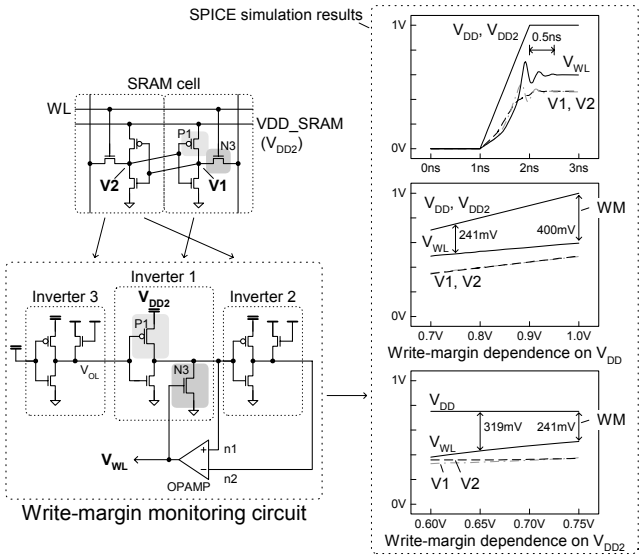

Figure 34.5.4: Proposed write-margin monitoring circuit.

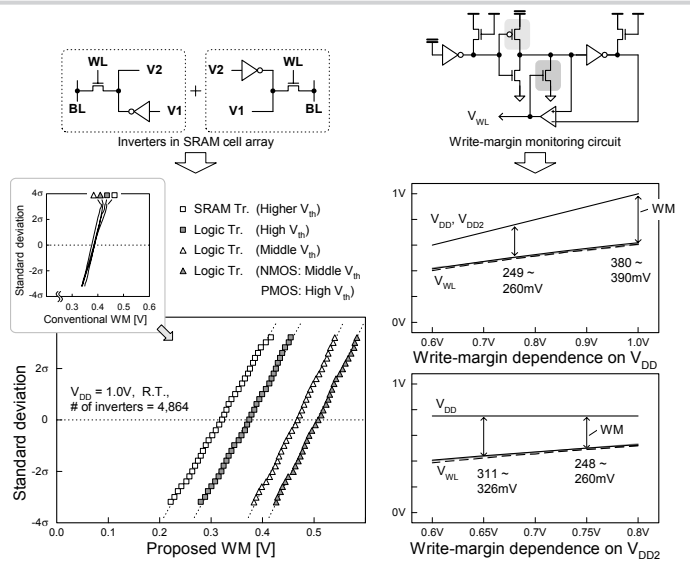

Figure 34.5.5: Measurement results.

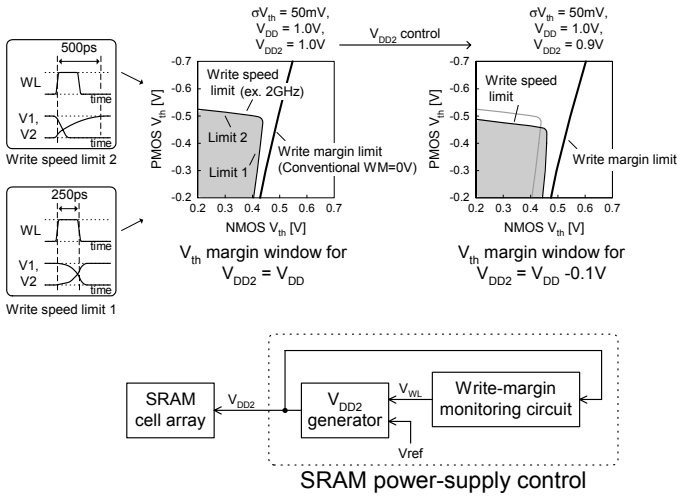

Figure 34.5.6: Application of write-margin monitoring circuit to SRAM power-supply control.

Continued on Page 678

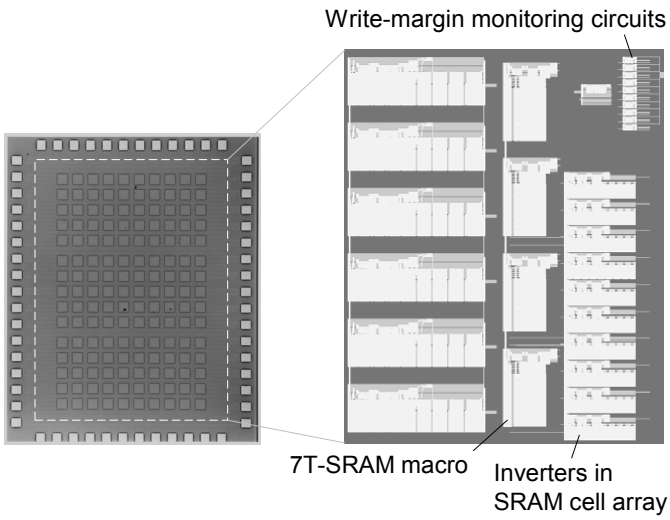

Figure 34.5.7: Chip micrograph and test-chip layout.

